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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/737,783	12/15/2000	Perry Wang	42390P9634	2478

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EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/737,783	WANG ET AL	
	Examin r	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sh et with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-13* is/are allowed.

6)☒ Claim(s) *1-8 and 14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims1-8 and 14-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

2. Claim 1 recites the limitation "the predicated instruction" on line 6 of claim 1. There is insufficient antecedent basis for this limitation in the claim.

3. Claims 1 and 14 recite the limitation "a plurality of registers defined by different predicates" on line 6 of claim 1. This is indefinite and unclear because "predicate" is defined as a declaration of either true or false, or a Boolean logic value. Thus, a plurality of registers cannot be defined by "predicates". Registers can be defined by "predicated instructions", however, that would determine the value stored in particular registers indicated by the instruction.

4. Claims 1 and 14 recite the limitation "a plurality of registers defined by different predicates upon which a common instruction depends" on line 6 of claim 1. This is indefinite because it is unclear which, or both, of the "plurality of registers" or the "different predicates" the "common instruction" depends. Without using commas, or other punctuation, or rewriting the limitation, the dependency is unclear and open for interpretation.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-8 and 14-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Gschwind et al, U.S. Patent Number 6,513,109 (herein referred to as Gschwind).

6. Referring to claim 1 Gschwind has taught a microprocessor comprising:

a unit to insert a first micro-operation into an instruction stream, the first micro-operation to defer renaming of a plurality of registers defined by different predicates upon which a common instruction depends (Gschwind column 2 lines 64-67, figures 2-3, column 16 lines 8-11, column 14 lines 19-26; figure 4 number 330, column 2 lines 9-23; out of order execution; column 6 lines 33-51, figure 11, predicting future register names and then later verifying the names – the verification is done after the execution, thus allowing the execution of the instruction without stalling for renaming, and then verifying before the instructions are retired – the verification, and correction to the renaming of registers if a prediction is wrong, is deferred till after the execution of the instruction);

a plurality of register renaming units to rename at least one register corresponding to the predicated instruction after the common instruction is executed (Gschwind figure 4 number 330; figure 4 number 330, column 2 lines 9-23; out of order execution; column 6 lines 33-51, figure 11, predicting future register names and then later verifying the names – the verification is done

after the execution, thus allowing the execution of the instruction without stalling for renaming, and then verifying before the instructions are retired);

an augmented register alias table (Gschwind column 10 lines 5-7, figure 10).

7. Referring to claim 2 Gschwind has taught wherein the register renaming unit renames each one of a plurality of source registers of the pipeline instruction and renames a destination register to a new physical register (Gschwind column 8 lines 25-43 figure 10).

8. Referring to claim 3 Gschwind has taught wherein the augmented register alias table includes a plurality of lines, and wherein each one of the plurality of lines includes a plurality of renamed destination registers (Gschwind figures 10-11, column 8 lines 25-43, column 9 line 65-column 10 line 32).

9. Referring to claim 4 Gschwind has taught wherein each one of a plurality of select-uops has a plurality of source operands wherein each one of the plurality of source operands corresponds to a physical register identifier (Gschwind figures 10-11, column 8 lines 25-43, column 9 line 65-column 10 line 32).

10. Referring to claim 5 Gschwind has taught wherein the plurality of source operands comprises a first source operand and a plurality of secondary source operands (Gschwind figure 10, the architected register names, and the future register names, column 9 line 65-column 10 line 32).

11. Referring to claim 6 Gschwind has taught wherein the first source operand includes a default physical register identifier, wherein the default physical register is always valid and available (Gschwind column 15 lines 48-65, column 14 line 46-column 15 line 28; the predicate register is a common register and is used for all predicate instructions and its always available).

12. Referring to claim 7 Gschwind has taught wherein each one of the plurality of secondary source operands includes a plurality of status bits and a physical register identifier (Gschwind figures 10-11, column 8 lines 25-43, column 9 line 65-column 10 line 32, column 22 lines 32-39).

13. Referring to claim 8 Gschwind has taught wherein each one of the plurality status bits has a ready bit and a committed bit (Gschwind column 17 lines 61-67, column 21 lines 7-12).

14. Referring to claim 14 Gschwind has taught a computer system comprising:

a processor, wherein the processor includes:

a unit to insert a first micro-operation into an instruction stream, the first micro-operation to defer renaming of a plurality of registers defined by different predicates upon which a common instruction depends (Gschwind column 2 lines 64-67, figures 2-3, column 16 lines 8-11, column 14 lines 19-26; figure 4 number 330, column 2 lines 9-23; out of order execution; column 6 lines 33-51, figure 11, predicting future register names and then later verifying the names – the verification is done after the execution, thus allowing the execution of the instruction without stalling for renaming, and then verifying before the instructions are retired – the verification, and correction to the renaming of registers if a prediction is wrong, is deferred till after the execution of the instruction);

a plurality of execution units to execute the dependent instruction (Gschwind figure 4 numbers 340, 345, 350);

a reorder buffer (Gschwind column 9 lines 55-58);

a plurality of register renaming units to rename at least one register corresponding to a predicated instruction after the dependent instruction is executed (Gschwind figure 4 number

330; figure 4 number 330, column 2 lines 9-23; out of order execution; column 6 lines 33-51, figure 11, predicting future register names and then later verifying the names – the verification is done after the execution, thus allowing the execution of the instruction without stalling for renaming, and then verifying before the instructions are retired);

a plurality of reservation stations wherein the register renaming unit, the reorder buffer, the plurality of execution units and the plurality of reservation stations are coupled to at least one of the plurality of dynamic pipeline stages (Gschwind figure 4 number 335); and

an augmented register alias table (Gschwind column 10 lines 5-7);

a system bus (Gschwind figure 4 the system bus would be the bus between the memory 305 and the cache systems);

a computer memory system (Gschwind 4 number 305);

an input/output device (Gschwind figure 4; most of the logical units are input and output devices, including the memory 305 and the data cache, the future register file, the execution units);

wherein the system bus is coupled to the processor, the computer memory system and the input/output device.

15. Referring to claim 15 Gschwind has taught wherein, the augmented register alias table includes a plurality of lines, and wherein each one of the plurality of lines includes a plurality of renamed destination registers (Gschwind figures 10-11, column 8 lines 25-43, column 9 line 65-column 10 line 32).

16. Referring to claim 16 Gschwind has taught wherein, the register renaming unit renames each one of the plurality of source registers of the pipeline instruction and renames the

destination register to a new physical register (Gschwind figures 10-11, column 8 lines 25-43, column 9 line 65-column 10 line 32).

Allowable Subject Matter

17. Claims 9-13 are allowed. The rejections of claims 9-13 have been withdrawn. In the remarks (third paragraph, page 8, filed 09/27/04), Applicant states that Gschwind does not teach the select-uop function, as stated in the claims, along with the teaching that the consumer instruction is executed using data from the destination registers of the select-uop, before the renaming of the destination register takes place.

Response to Arguments

18. Applicant's arguments, filed 09/27/04, with respect to claim 9-13 have been fully considered and are persuasive. The rejections of claims 9-13 have been withdrawn. In the remarks (third paragraph, page 8, filed 09/27/04), Applicant states that Gschwind does not teach the select-uop function, as stated in the claims, along with the teaching that the consumer instruction is executed using data from the destination registers of the select-uop, before the renaming of the destination register takes place.

19. Applicant's arguments, filed 09/27/04, with respect to claims 1-8 and 14-16 have been considered but are not persuasive. Claims 1-8 and 14-16 are rejected as being indefinite and unclear, as stated above. In the current state, the Examiner believes that Gschwind still anticipates these claims by leaving the renaming of the register after the execution of the

instruction that depends on the register, by first predicting the register renaming, and then verifying and/or correcting the register renaming after execution is complete, and uses predicate registers and logic during execution.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 571-272-4167. The examiner can normally be reached on 9Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Allen Harkness

Examiner

Art Unit 2183

December 20, 2004

RICHARD L. ELLIS
PRIMARY EXAMINER